EMIF02-600FU7

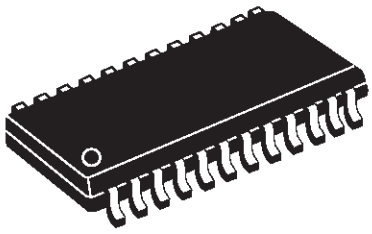
Application Specific Discretes
A.S.D.™

10-BIT WIDE EMI FILTER INCUDING ESD PROTECTION

MAIN APPLICATIONS

Where EMI filtering in ESD sensitive equipment is required :

- Computers and printers
- Communication systems
- Mobile phones
- MCU Boards



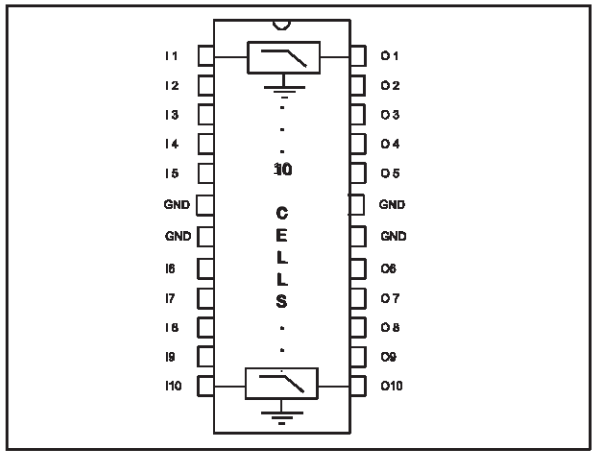
SSOP24

DESCRIPTION

The EMIF02-600FU7 is a highly integrated array designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences.

Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV. The EMIF02-600FU7 provides best efficiency when using separated inputs and outputs, in the so-called 4-points structure.

FUNCTIONAL DIAGRAM



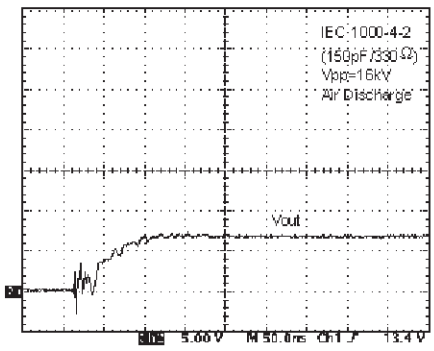
BENEFITS

- 10-bit EMI bi-directional low-pass-filter
- Enhanced ESD protection for the protected device, optimized by the four point structure
- High flexibility in the design of high density boards

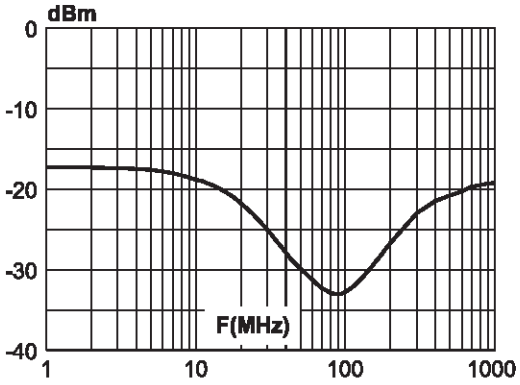
COMPLIES WITH THE FOLLOWING STANDARDS :

IEC 1000-4-2	15kV	(air discharge)
	8 kV	(contact discharge)

ESD response to IEC1000-4-2 (15 kV air discharge)



Filtering response (with 50Ω line)



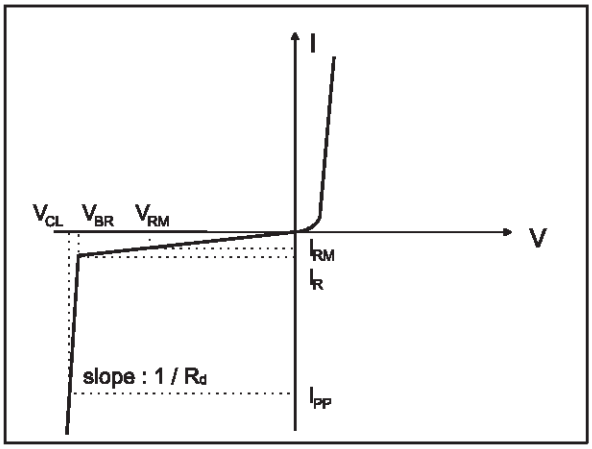
TM : ASD is trademark of STMicroelectronics.

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C)

Symbol	Parameter and test conditions	Value	Unit
V_{PP}	ESD discharge IEC1000-4-2, air discharge ESD discharge IEC1000-4-2, contact discharge	16 9	kV
T_j	Junction temperature	150	°C
T_{op}	Operating temperature range	-40 to + 85	°C
T_{stg}	Storage temperature range	-55 to +150	°C
T_L	Lead solder temperature (10 second duration)	260	°C

ELECTRICAL CHARACTERISTICS (T_{amb} = 25 °C)

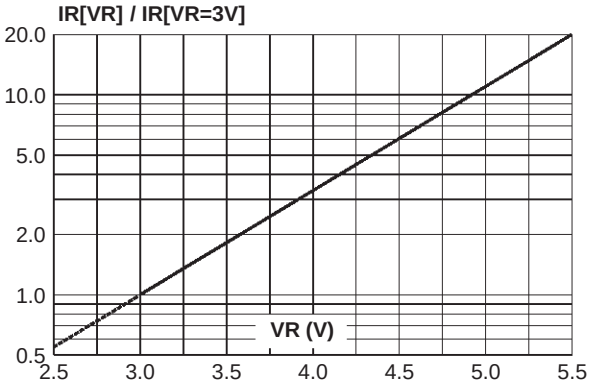
Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
Rd	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Serial resistance between Input and Output



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6	7	8	V
I_{RM}	V_{RM} = 3V			1	µA
$R_{I/O}$	Serial resistance between Input and Output	480	600	720	Ω
R_d	I_{pp} = 10 A, t_p = 2.5 µs (see note 1)		0.55		Ω

Note 1 : to calculate the ESD residual voltage, please refer to the paragraph "ESD PROTECTION" on pages 4 & 5

Fig.1 : Relative variation of leakage current versus reverse voltage (Typical values)



TECHNICAL INFORMATION

FREQUENCY BEHAVIOR

The EMIF02-600FU7 is firstly designed as an EMI/RFI filter. This low-pass filter is characterized by the following parameters:

- Cut-off frequency
- Insertion loss
- High frequency rejection

Fig A1 : EMIF02-600FU7 frequency response curve.

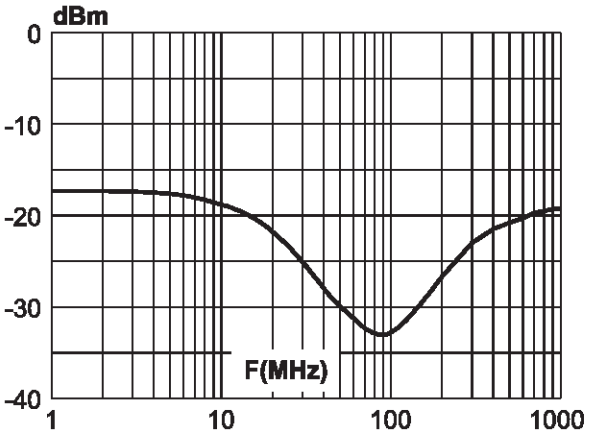
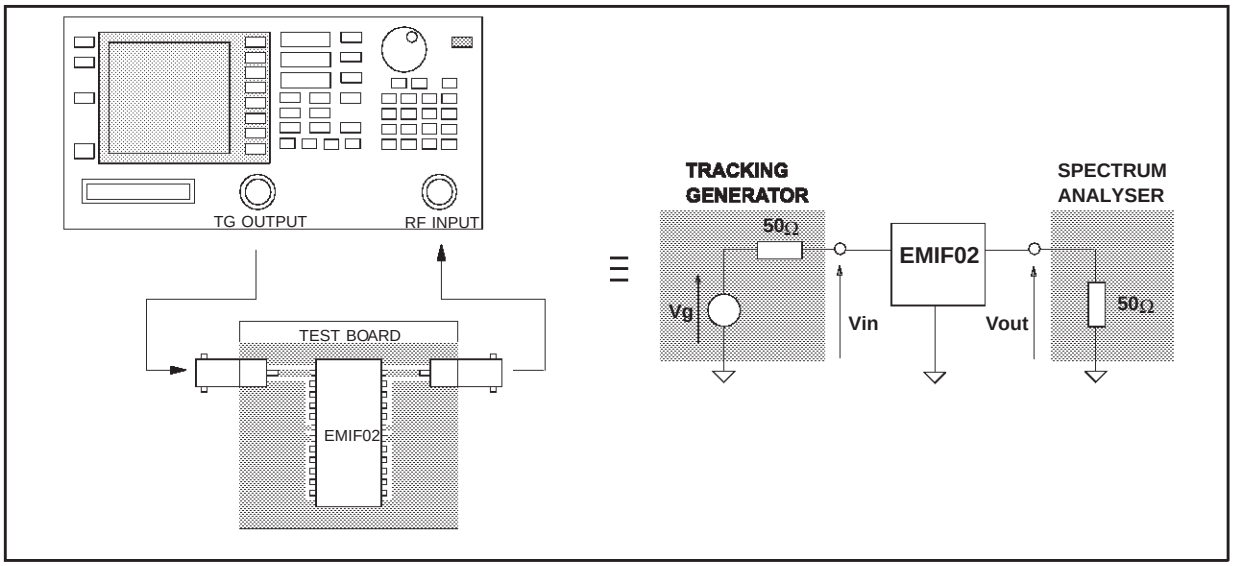


Figure A1 gives these parameters, in particular the signal rejection at the GSM frequency is about -20dBm at 900MHz, while the attenuation for FM broadcast range (around 100MHz) is better than -32dBm

Fig A2 : Measurement conditions



ESD PROTECTION

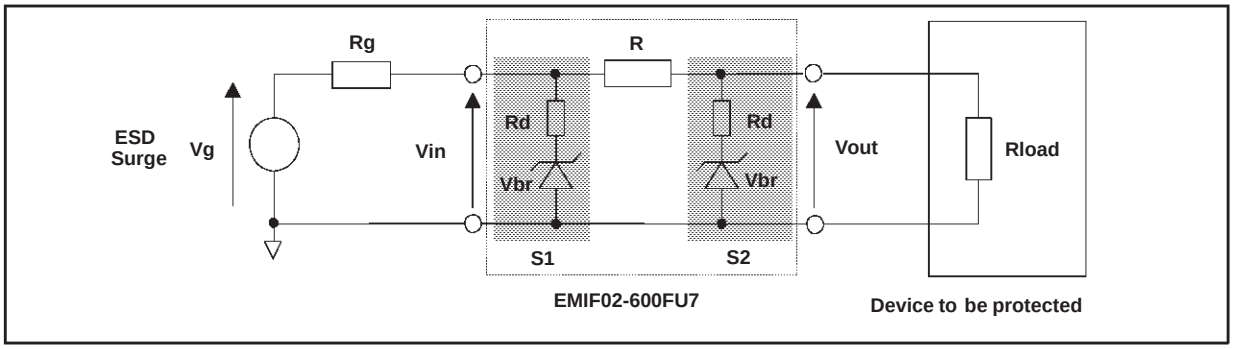
In addition to its filtering function, the EMIF02-600FU7 is particularly optimized to perform ESD protection.

ESD protection is based on voltage clamping which can be calculated by :

$$V_{CL} = V_{BR} + R_d.I_{PP}$$

This protection function is splitted in 2 stages. As shown in figure A3, the ESD strikes are clamped by the first stage S1 and then its remaining overvoltage is applied to the second stage through the resistor R. Such a configuration makes the output voltage V_{out} very low.

Fig A3 : ESD clamping behavior



To have a good approximation of the remaining voltages at both Vin and Vout stages, we provide the typical dynamical resistance value Rd. By taking into account these following hypothesis : R>>Rd, R_G>>Rd and Rload>>Rd, it gives these formulas:

$$Vin = \frac{Rg.Vbr + Rd.Vg}{Rg}$$

$$Vout = \frac{R.Vbr + Rd.Vin}{R}$$

The results of the calculation done for V_G=8kV, R_G=330Ω (IEC1000-4-2 standard) and V_{BR}=7V (typ.) give:

$$Vin = 20.33\,V$$

$$\underline{\mathbf{Vout = 7.01\ V}}$$

This confirms the very low remaining voltage across the device to be protected. It is also important to note that in this approximation the parasitic inductance effect was not taken into account. This could be few tenths of volts during few ns at the Vin side. This parasitic effect is not present at the Vout side due the low current involved after the resistance R.

The measurements shown here after illustrate very clearly (Fig. A5a) the high efficiency of the ESD protection :

- no influence of the parasitic inductances on Vout stage
- Vout clamping voltage very close to V_{BR}

Fig A4 : Measurement conditions

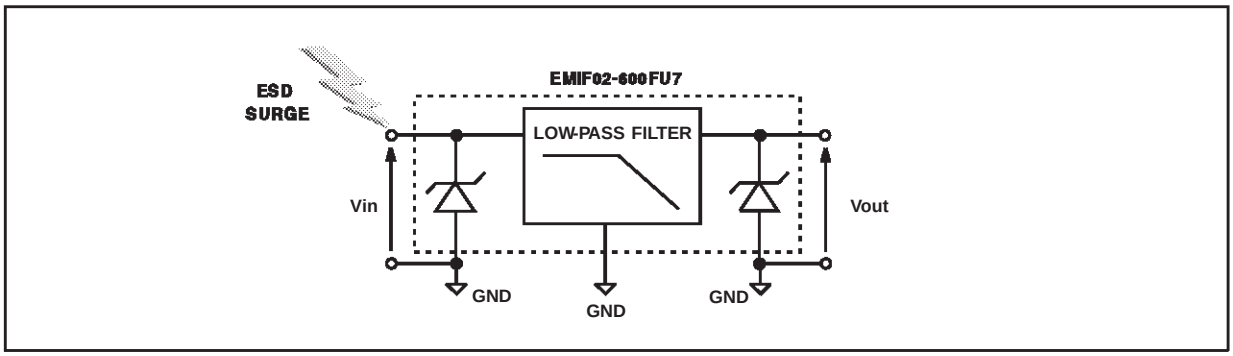
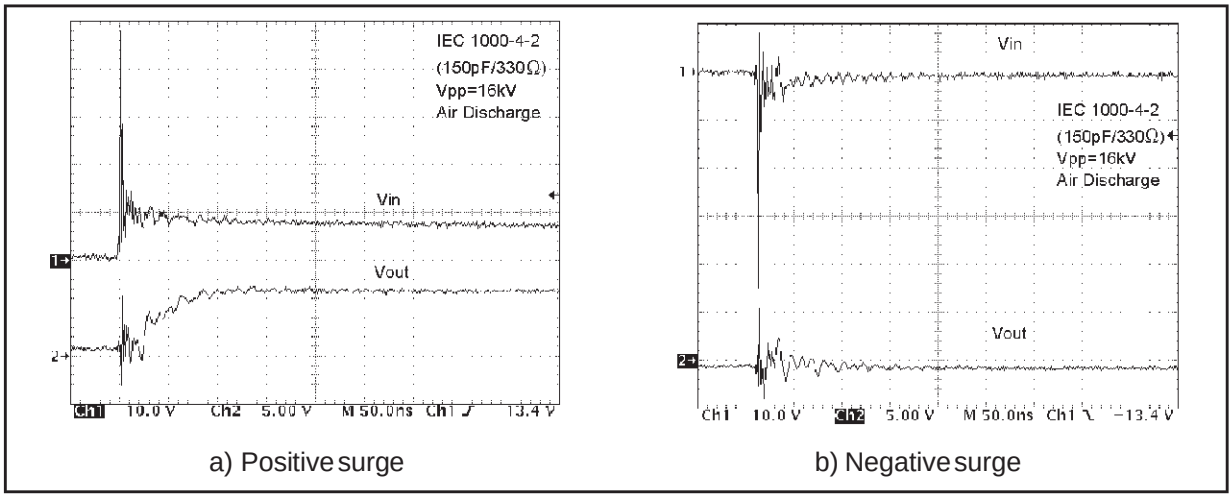


Fig A5 : Remaining voltage at both stages S1 (Vin) and S2 (Vout) during ESD surge



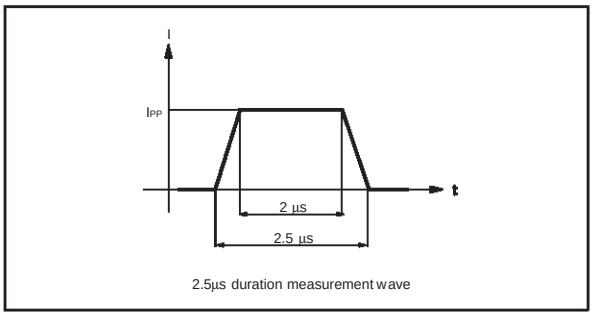
a) Positive surge b) Negative surge

Please note that the EMIF02-600FU7 is not only acting for positive ESD surges but also for negative ones. For these kind of disturbances it clamps close to ground voltage as shown in Fig. A5b.

NOTE: DYNAMIC RESISTANCE MEASUREMENT

As the value of the dynamic resistance remains stable for a surge duration lower than 20µs, the 2.5µs rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd.

Fig A6 : Rd measurement current wave

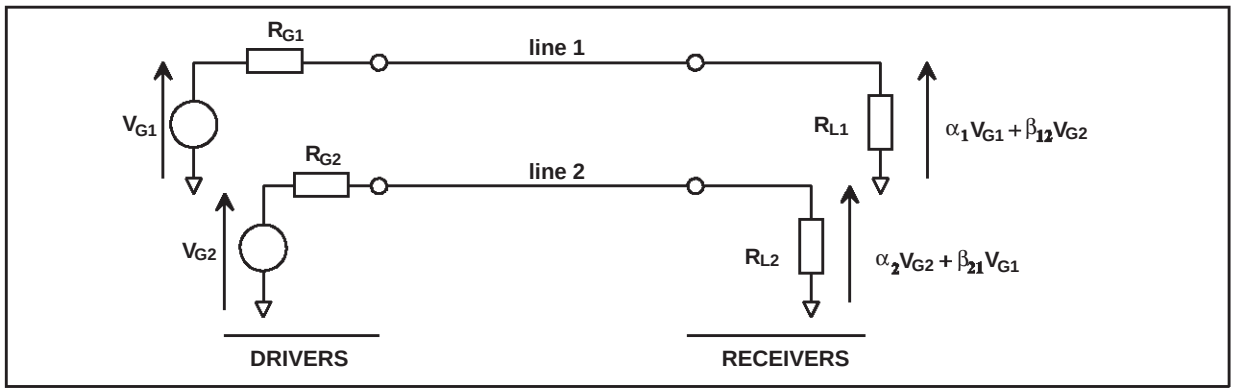


2.5µs duration measurement wave

CROSSTALK BEHAVIOR

1- Crosstalk phenomena

Fig A7 : Crosstalk phenomena



The crosstalk phenomena are due to the coupling between 2 lines. The coupling factor (β_{12} or β_{21}) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load R_{L2} is $\alpha 2V_{G2}$, in fact the real voltage at this point has got an extra value $\beta 21V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few kΩ). The following chapters give the value of both digital and analog crosstalk.

2- Digital Crosstalk

Fig A8 : Digital crosstalk measurement

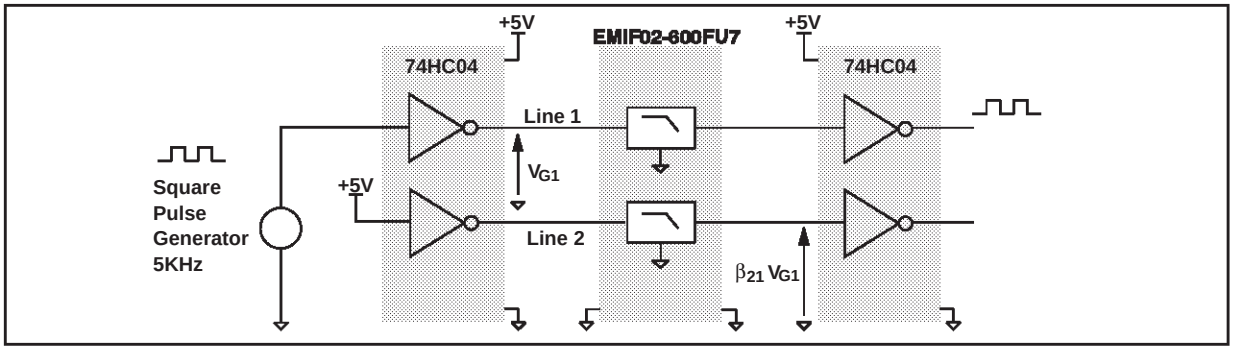
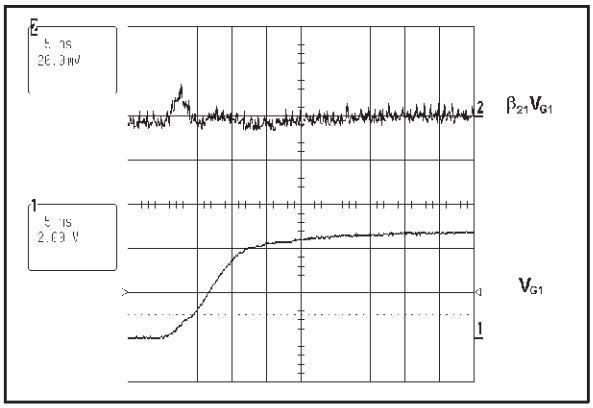


Figure A8 shows the measurement circuit used to quantify the crosstalk effect in a classical digital application.

Figure A9 shows that in such a condition signal from 0 to 5V and rise time of 10 ns, the impact on the disturbed line is less than 20mV peak to peak. No data disturbance was noted on the concerned line. The same results were obtained with falling edges.

Fig A9 : Digital crosstalk results



3- Analog Crosstalk

Fig A10 : Analog crosstalk measurement

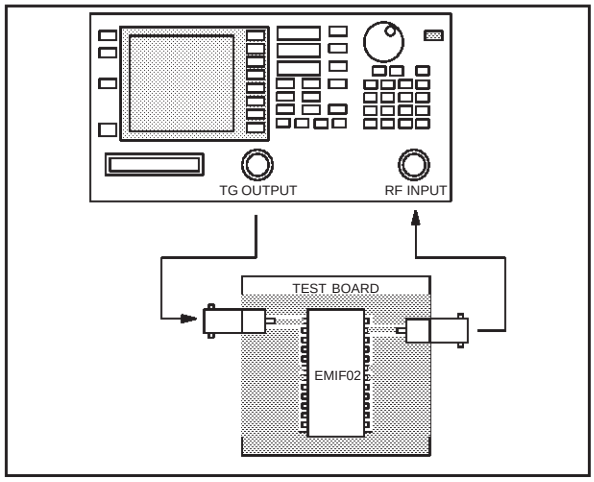


Fig A11 : Typical analog crosstalk result

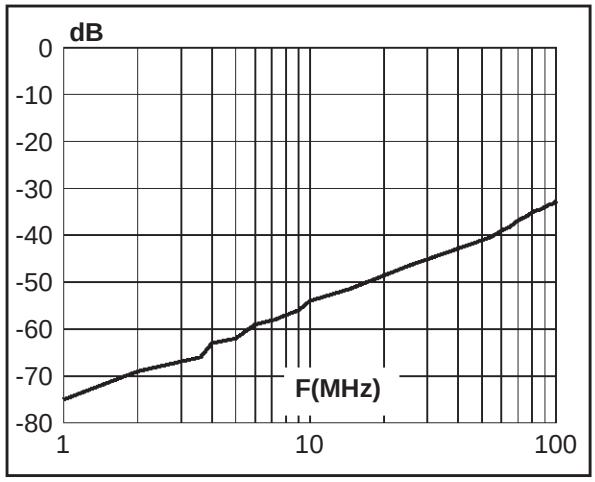


Figure A10 gives the measurement circuit for the analog application. In figure A11, the curve shows the effect of cell 1/24 on cell 2/23, no difference was found with other couples of adjacent cells. In usual frequency range of analog signals (up to 100MHz) the effect on disturbed line is less than -32 dBm.

PSPICE MODEL

Fig A12 : PSpice model of one EMIF02-600FU7 cell

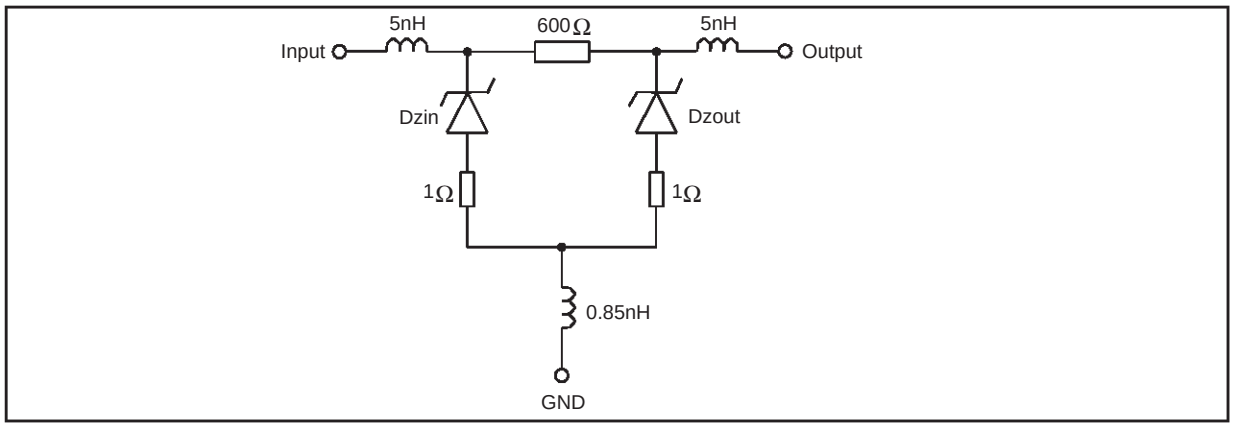


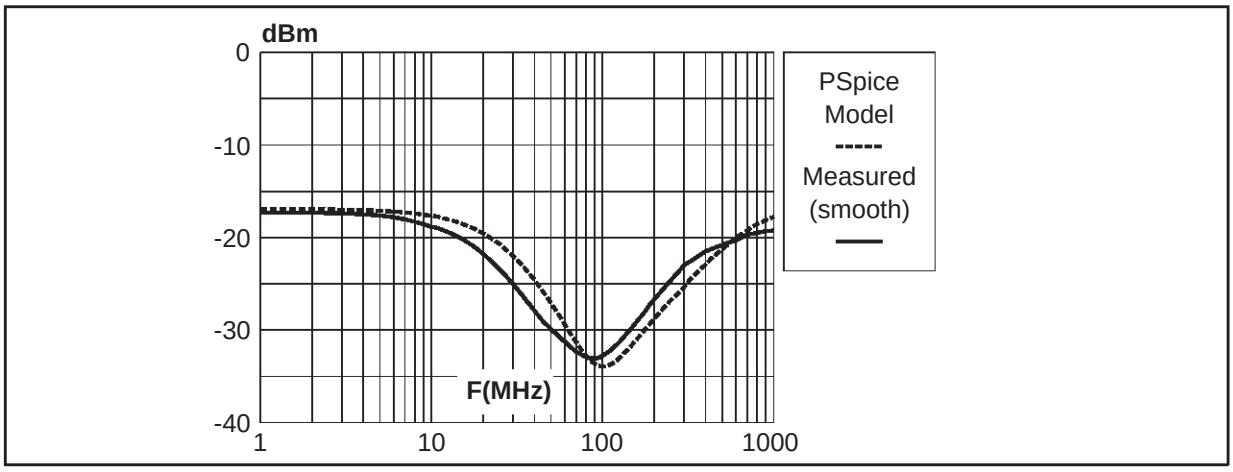
Figure A12 shows the PSpice model of one cell of the EMIF02-600FU7. In this model, the clamping diodes (Dzin and Dzout) are defined by the following PSpice parameters :

RS = 0.55
Cjo = 100p
M = 0.3333
VJ = 0.6
BV = 7
IBV = 1u

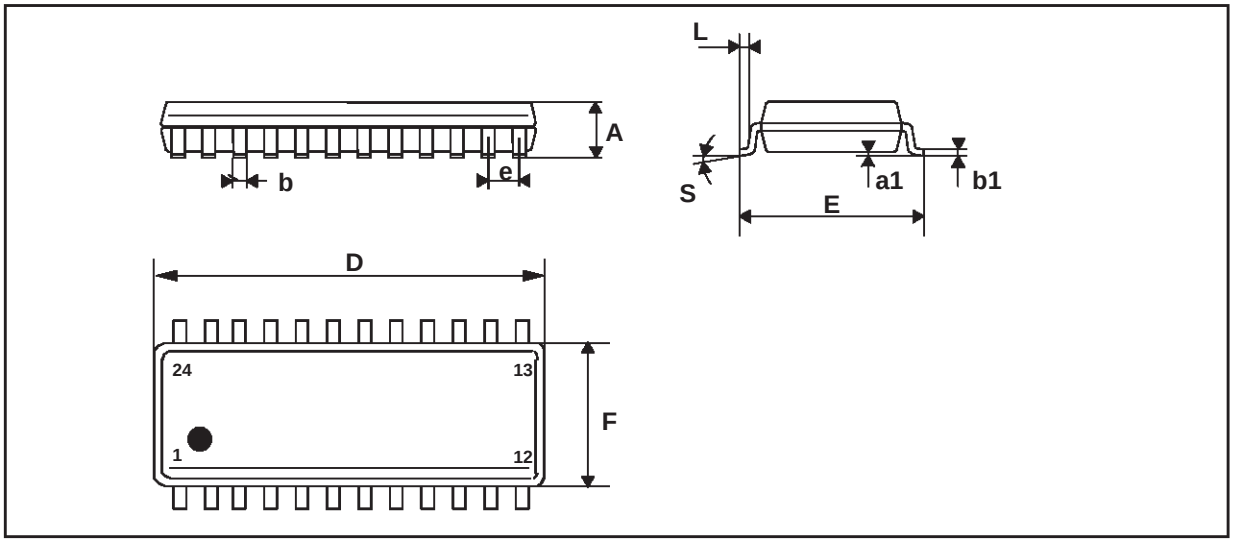
This model is available for frequency simulation and for ambient temperature of 27°C.

The comparison between the PSpice simulation and the measured frequency response is given in figáA13. This shows that the PSpice model is very close to the product behavior.

Fig A13 : Comparison between PSpice simulation and measured frequency response



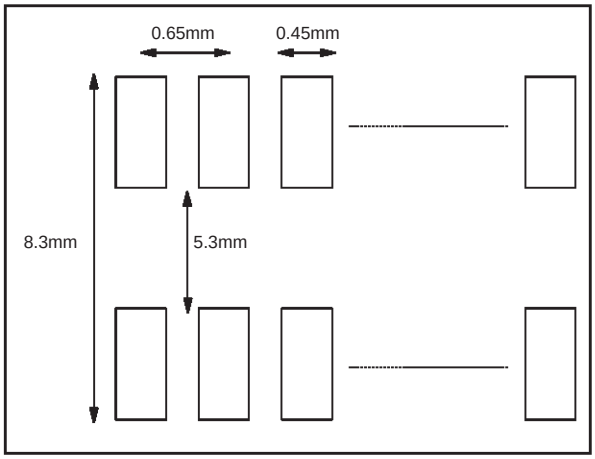
PACKAGE MECHANICAL DATA
SSOP24



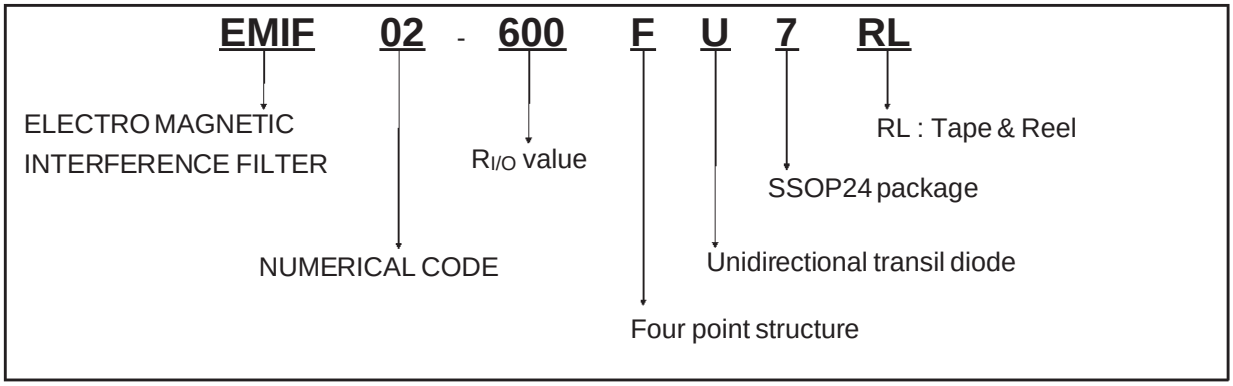
REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.73	1.86	2.00	0.068	0.073	0.079
a1	0.05		0.25	0.002		0.010
b	0.25		0.35	0.010		0.014
b1	0.10		0.35	0.0035		0.014
D	8.07	8.20	8.33	0.317	0.322	0.328
E	7.60		7.90	0.299		0.311
e		0.65			0.0256	
F	5.20		5.38	0.2047		0.2118
L	0.25		0.88	0.010		0.0347
S	8° max					

Mechanical specifications	
Lead plating	Tin-lead
Lead plating thickness	7µm min. 20 µm max.
Lead material	Copper alloy
Lead coplanarity	0.08mm max.
Body material	Molded epoxy
Flammability	UL94V-0

RECOMMENDED FOOTPRINT



ORDER CODE



Order code	Marking	Package	Weight	Base qty	Delivery mode
EMIF02-600FU7	EMIF02-600	SSOP24	0.19g	59	tube
EMIF02-600FU7RL	EMIF02-600	SSOP24	0.19g	2000	tape & reel